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BY: Amelia C. Nearing

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SPECIFICATION

To all whom it may concern:

Be It Known, That I, **Jeffrey Scott Brown, a citizen of the United States of America, residing at 3624 Goodell Lane, Fort Collins, Colorado 80526**, have invented certain new and useful improvements in **"Type Configurable Memory Methodology for Use with Metal Programmable Devices"**, of which I declare the following to be a full, clear and exact description:

BACKGROUND OF THE INVENTION

1. Technical Field:

The present invention is directed generally toward metal programmable devices and, more particularly, to a method and apparatus for providing type configurable memory in a metal programmable device.

2. Description of the Related Art:

In recent years, there has been a growth in products in which semi-custom techniques are used. Application-specific integrated circuits (ASIC) are widely used in consumer, manufacturing, communications, and amusement products, as well as other applications where a specific circuit may be needed. ASICs are very useful in bringing unique, customer-specific products to market on time.

The gate array is an example of an ASIC. Gate arrays are arrays of elements, such as AND or NAND gates, although today the term "gate array" usually refers to an array of transistors. These transistors can be tightly packed on an integrated circuit and later connected with a metal layer to form the application-specific circuit. These are referred to as metal programmable devices.

As gate array products became more sophisticated, it became necessary to form a memory in the circuit. Memory cells may be formed from the gate array transistors themselves. This approach is very flexible, because any number of memory cells of any type can be formed, within the area limitations in the gate array. However, each memory cell uses several transistors and a memory core may take up an undesirable amount of area and transistors in the gate array.

Another solution is to embed a memory in the gate array chip. Memory cells may be fabricated much more densely than memory cells formed from transistors in the gate array. Interface logic is also provided for the application-specific circuit to access the memory core. This solution allows much more memory to be provided in a smaller area. However, the type of memory is fixed in the gate array product. Therefore, if a single port memory is provided and the application-specific circuit requires a dual port memory, it will not be possible to produce the

application-specific circuit with the gate array product.

Therefore, it would be advantageous to provide type configurable memory in a metal programmable device.

SUMMARY OF THE INVENTION

The present invention provides a pre-diffused array of core memory cells in a metal programmable device and multiple control block versions of interface logic. The memory interface logic is placed around the memory core. Contact points for each control block are brought to the surface of the wafer using a via. The appropriate interface logic is selected by connecting the metal layer to the appropriate surface contacts to access the core memory cells. The application-specific circuit, including memory configuration and memory interface type, is programmed with the metal layer.

BRIEF DESCRIPTION OF THE DRAWINGS

The novel features believed characteristic of the invention are set forth in the appended claims. The invention itself however, as well as a preferred mode of use, further objects and advantages thereof, will best be understood by reference to the following detailed description of an illustrative embodiment when read in conjunction with the accompanying drawings, wherein:

Figures 1A-1C, a block diagram of an example metal programmable device, is depicted in accordance with a preferred embodiment of the present invention;

Figures 2A and **2B**, diagrams illustrating cross sections of a metal programmable device, are shown in accordance with an exemplary embodiment of the present invention;

Figure 3 is a flowchart illustrating the operation of providing a metal programmable device with flexible embedded memory in accordance with a preferred embodiment of the present invention; and

Figure 4 shows a flowchart illustrating the operation of providing an application-specific circuit using the metal programmable device of the present invention.

DETAILED DESCRIPTION

The description of the preferred embodiment of the present invention has been presented for purposes of illustration and description, but is not intended to be exhaustive or limited to the invention in the form disclosed. Many modifications and variations will be apparent to those of ordinary skill in the art. The embodiment was chosen and described in order to best explain the principles of the invention the practical application to enable others of ordinary skill in the art to understand the invention for various embodiments with various modifications as are suited to the particular use contemplated.

With reference now to the figures and in particular with reference to **Figures 1A-1C**, a block diagram of an example metal programmable device is depicted in accordance with a preferred embodiment of the present invention. More particularly, with reference to **Figure 1A**, metal programmable device **100** includes gate array cells **130** and memory core array **110**. In an exemplary embodiment, the gate array is made up of "Rcells." Each Rcell is a five-transistor cell, which includes two NMOS and two PMOS devices, and one small PMOS device. An application-specific circuit can be formed by programming the gate array cells with a metal layer. This circuit may use the memory core array to store and retrieve data.

The memory core is made up of versatile bitcells. An example of a versatile bitcell is the 6T static random access memory (SRAM) cell, as shown in **Figure 1B**. Memory interface logic **120** is wrapped around the memory core. These multiple control logic versions may be used to access the memory as different types, using the same base bitcell. Each control block version will always be present around the memory core; however, only the desired memory interface(s) may be connected through upper level contact using metal programming.

Figure 1C is a block diagram illustrating a memory interface logic in accordance with a preferred embodiment of the present invention. Memory interface logic **120** includes control blocks **122**, **124**, **126**. Each control block includes components that are pre-diffused in the device. These control blocks include components that make up memory interface logic of different types. In the depicted example, three control blocks are shown; however, more or fewer control blocks may be included depending upon the implementation. Ideally, the memory

interface logic will include as many control blocks as there are memory types supported by the base memory cell. Memory interface logic **120** may also include components in area **128** that are common to multiple control blocks. For example, all control blocks may share a set of sense amps or the like.

As an example, memory interface logic **122** may access the memory as a typical 6T single port SRAM with each access triggered on the rising edge of the clock. Memory interface logic **124** may access the memory as a pseudo 211 (dual port, single read port, single write port) type memory, performing a read on each rising edge of the clock and a write on each falling edge of the clock. The same memory cells may be accessed by memory interface logic **126** in a read only memory (ROM) mode where the 6T cells are also tied/programmed in an upper level layer using metal programming. Thus, in this example, if the customer logic calls for a single port memory, a metal layer may be applied to connect control block **122** to the memory core. Furthermore, any combinations of memory interface control blocks may be connected to the memory core to access subsets of the memory cells. Therefore, parts of the customer logic may access a first portion of the memory core as a first memory type and other parts of the customer logic may access a second portion of the memory core as a second type.

With reference to **Figures 2A** and **2B**, diagrams illustrating cross sections of a metal programmable device are shown in accordance with an exemplary embodiment of the present invention. More particularly, with reference to **Figure 2A**, substrate **200** includes components **222**, **224**, **226**, **228** and memory cell **210**. Connection to components **222-228** may be made through contacts **232**, **234**, **236**, **238**. Contact points are brought to the surface of the substrate using a via.

As an example, component **222** may belong to a first control block in a memory interface logic, component **224** may belong to a second control block, and component **226** may belong to a third control block. Component **228** may be common to two or more control blocks. For example, component **228** may be used by the first control block and the second control block. Contract **212** may be used to connect memory cell **210** to other components, particularly memory interface logic.

Turning to **Figure 2B**, metal layer **250** connects component **226** to memory cell **210**. Metal layer **250** may connect many other components within the memory interface logic. The metal layer provides a configuration of "painted" metal lines connecting device logic, interface logic, and/or memory cells. Using this metal layer, an application specific device may be configured from the programmable device of the present invention. Such a device may include a versatile memory core that may be accessed as different types of memory, depending upon the particular memory interface control blocks that are connected using the metal layer.

Figure 3 is a flowchart illustrating the operation of providing a metal programmable device with flexible embedded memory in accordance with a preferred embodiment of the present invention. The process begins and provides logic cells with area reserved for memory cells and area reserved for memory interface logic (step **302**). Then, the process provides configurable memory cells in the reserved area of the metal programmable device (step **304**). Thereafter, the process provides multiple type memory control logic around the memory cells in the metal programmable device (step **306**) and the process ends.

Next, **Figure 4** shows a flowchart illustrating the operation of providing an application-specific circuit using the metal programmable device of the present invention. The process begins and configures the customer logic (step **402**). Then, the process determines a memory type for the memory interface control logic (step **404**). Next, the process applies a metal layer to program the customer logic and to connect the appropriate memory interface control logic to the memory cells (step **406**). Thereafter, the process ends.

Thus, the present invention solves the disadvantages of the prior art by providing a pre-diffused array of core memory cells in a metal programmable device and multiple control block versions of interface logic. The memory interface logic is placed around the memory core. Contact points for each control block are brought to the surface of the wafer using a via. The appropriate interface logic is selected by connecting the metal layer to the appropriate surface contacts to access the core memory cells. The application-specific circuit, including memory configuration and memory interface type, is programmed with the metal layer.